

U.S. Patent Application Serial No. 10/027,856  
Reply to Office Action mailed November 5, 2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 1, 7, and 12 are amended.

**Listing of Claims:**

1. (Currently Amended) A semiconductor device comprising:  
a die-pad including a first surface, a second surface opposite to the first surface, and a peripheral edge, the second surface including an exposed portion and a retreated portion around the exposed portion;  
a semiconductor chip mounted on the first surface of the die-pad; and  
a sealing resin covering the die-pad and the semiconductor chip, the resin allowing the exposed portion to be exposed and being held in contact with the retreated portion,  
wherein the die-pad is formed with at least one slit that is open in the retreated portion of the second surface and in the first surface,  
the at least one slit is located between the peripheral edge of the die-pad and the semiconductor chip,  
the semiconductor chip has a side facing the at least one slit and extending from a first corner of the chip to a second corner of the chip, and  
the at least one slit is formed along the side of the chip and extends continuously from a first position that is closer to the first corner of the chip than to the second corner of the chip, to a second position that is closer to the second corner of the chip than to the first corner of the chip.
2. (Original) The semiconductor device according to claim 1, wherein the retreated portion is defined by a retreated surface and a side surface which adjoins the exposed portion and forms an acute angle together with the retreated surface.

U.S. Patent Application Serial No. 10/027,856  
Reply to Office Action mailed November 5, 2004

3. (Canceled)

4. (Previously Presented) The semiconductor device according to claim 1, wherein the die-pad is formed with a plurality of slits that are open in the retreated surface of the second surface and in the first surface, the plurality of slits being arranged to surround the semiconductor chip.

5. (Previously Presented) The semiconductor device according to claim 1, wherein the semiconductor chip is electrically connected to the die-pad via a first wire, the first wire being connected to the first surface of the die-pad at a portion between the peripheral edge of the die-pad and the at least one slit.

6. (Original) The semiconductor device according to claim 1, further comprising a terminal electrically connected to the semiconductor chip via a second wire, the terminal being retained by the sealing resin so as to be partially exposed.

7. (Currently Amended) A semiconductor device comprising:

a semiconductor chip;

a die-pad including an upper surface on which the semiconductor chip is mounted and a lower surface opposite to the first surface, the die-pad being electrically connected to the semiconductor chip via a first wire;

a plurality of leads spaced from the die-pad via a clearance and electrically connected to the semiconductor chip via second wires; and

a sealing resin enclosing the semiconductor chip in a manner such that the lower surface of the die-pad is exposed;

wherein the die-pad includes a thin-walled portion formed by removing a part of the lower surface along a peripheral edge of the die-pad, the die-pad being formed with at least one slit extending through the thin-walled portion,

U.S. Patent Application Serial No. 10/027,856  
Reply to Office Action mailed November 5, 2004

the at least one slit is located inwardly from the clearance and between the peripheral edge of the die-pad and the semiconductor chip,

the semiconductor chip has a side facing the at least one slit and extends from a first corner of the chip to a second corner of the chip, and

the at least one slit is formed along the side of the chip and extend~~ed~~s continuously from a first position that is closer to the first corner of the chip than to the second corner of the chip, to a second position that is closer to the second corner of the chip than to the first corner of the chip.

8. (Original) The semiconductor device according to claim 7, wherein the sealing resin extends under the thin-walled portion so as not to expose an opening of the slit.

9. (Previously Presented) The semiconductor device according to claim 8, wherein the at least one slit extends along at least one side surface of the semiconductor chip around the semiconductor chip.

10. (Previously Presented) The semiconductor device according to claim 8, wherein the first wire is connected at one end thereof to the semiconductor chip and connected at another end thereof to the die-pad at a portion between the peripheral edge of the die-pad and the at least one slit.

11. (Canceled)

12. (Currently Amended) A semiconductor device comprising:

a die-pad including a first surface, a second surface opposite to the first surface, and a peripheral edge, the second surface including an exposed portion and a retreated portion around the exposed portion;

U.S. Patent Application Serial No. 10/027,856  
Reply to Office Action mailed November 5, 2004

a semiconductor chip mounted on the first surface of the die-pad, the chip having a first side and a second side adjoining the first side to define a corner between the first and second sides; and

a sealing resin covering the die-pad and the semiconductor chip, the resin allowing the exposed portion to be exposed and being held in contact with the retreated portion,

wherein the die-pad is formed with ~~a plurality of~~ first and second slits each of which is open in the retreated surface of the second surface and in the first surface,

the slits are being located between the peripheral edge of the die-pad and the semiconductor chip,

the first slit[[s face]]facing and extending along the first side and second side,  
~~respectively,~~ of the semiconductor chip, the second slit facing and extending along the second side of the semiconductor chip, and

wherein the ~~plurality~~ first and second [[of]] slits are discontinuous with each other at the corner of the chip.